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A Power Aware Two Direction Error Correction and Detection Technique

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Abstract: This paper develops the error correction and detection method for Power aware error correction and detection and Increase the number of errors that can be detected and corrected in power state of digital communication devices. Consequence of this research can used in wireless sensors and IOT components because the prudence of power is important. This Method will dynamically change the method of error correction and detection based on power state of machine. Error correction and detection method that used is two dimensional error correction and detection based on hamming code. The circuits that create the redundancy bits and control of errors that maybe happened are simulated.

Keywords: Error correction and Detection, Two dimensional Hamming code, Dynamic power consumption.

I. INTRODUCTION

History of error correction and detection will be discussed. This paper study about a new two dimensional hamming error correction and detection. Redundant circuit for error correction of this method increase the power consumption of sender and receivers and is a problem in the sender and receiver circuits. It is important that we should decrease the power consumption in the confidence systems. In dynamic power aware systems it is possible to control amount of used power base on source power and make it better as a time function. Other method for error correction or detection used for example cyclic redundant check (CRC), checksum and gray codes are used in digital systems but mentioned methods can detect only but cannot to correct error bit(s).

II. REVIEW OF LITERATURE

The hamming cod was submitted by hamming in Bell Lab of United States at April 1945. Hamming increase k redundancies bit to m bit of message Based on equation (1). This equation is a general equation and for hamming code, that can correct only one error bit then n is equal one and K is the number of redundant bits and m is number of data bits. Therefor the standard hamming code have m+k bit at all. In this case the equation (2) was achieved.

$$\sum_{i=0}^{n}\binom{m+k}{i} \le 2^k \qquad (1)$$

Based on equation (2) the number of redundancy k bit is calculated. K bit is the minimum number of bits that must be added to data bits for one bit error correction be possible by hamming code hence distance of hamming will be 3 after increase the number of bits from m to m+k bits. This is shown in figure (1). By selecting m=8 then amount of k is 4 from equation (2).

$$\sum_{i=0}^{n}\binom{m+k}{i} \le 2^k \Rightarrow \sum_{i=0}^{n=1}\binom{m+k}{i} \Rightarrow$$

$$m+k+1 \le 2^k \qquad (2)$$

P 1	P 2	M 3	P 4	M 5	M 6	M 7	P 8	M 9	M 10	M 11	M 12

Figure (1) -Hamming code structure (m=8 bits for message an k=4 bits for redundancy)

In figure (1) the p_{2^i} are redundancy and calculated by equation (3).

$$P1 = m3 \oplus m5 \oplus m7 \oplus m9 \oplus m11$$
$$P2 = m3 \oplus m6 \oplus m7 \oplus m10 \oplus m11$$
$$P4 = m5 \oplus m6 \oplus m7 \oplus m12$$
$$P8 = m9 \oplus m10 \oplus m11 \oplus m12 \qquad (3)$$

Pi is parity redundancy bit and mi is message bit in equation (3). And equation (4) used for error correction state that done in receiver.

$$C1 = P1 \oplus m3 \oplus m5 \oplus m7 \oplus m9 \oplus m11$$
$$C2 = P2 \oplus m3 \oplus m6 \oplus m7 \oplus m10 \oplus m11$$
$$C4 = P4 \oplus m5 \oplus m6 \oplus m7 \oplus m12$$
$$C8 = P8 \oplus m9 \oplus m10 \oplus m11 \oplus m12 \qquad (4)$$

It is possible that calculate error location bit by equation (5).

$$\text{Error Location Index} = (8 * P8 + 4 * P4 + 2 * P2 + P1) \qquad (5)$$

The error location bit is calculated by (5) equation. Error location calculate and hand in to decoder and index of error bit will export to error correction circuit and save to buffer. Error bit change after error location detected

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III.TWO DIMENSIONAL ERROR DETECTION AND CORRECTION.

We calculate the parity bits of hamming and move those bits to left corner of message bits that shown in figure (2).

P 1	P 2	P 4	P 8	M 3	M 5	M 6	M 7	M 9	M 10	M 11	M 12

Figure (2). Moving parity bit to left corner Messages bits in figure (2) are linier format that we know as one dimensional method. it is possible that the data by linier format store by matrix format and hamming code calculated in both dimension and place in corner of data. Two diminution data show in figure (3).

M11	M12	M13	M14	M15	M16	M17	M18
M21	M22	M23	M24	M25	M26	M27	M28

M31	M32	M33	M34	M35	M36	M37	M38
M41	M42	M43	M44	M45	M46	M47	M48
M51	.	.	.	.	.	.	M58
M61	.	.	.	.	.	.	M68
M71	.	.	.	.	.	.	M78
M81	M82	M83	M84	M85	M86	M87	M88

Figure (3). Two dimension message bits

By placing of parity bits in left corner and down corner of data after calculate of row and column parity figure (4) show this state. Parity bits are Pi and Qi in row and column.

Pi and Qi parity bits will be stored in memory and send with serial method. In this case if a row or column of data bits have errors then Pi and Qi parity bits only see a bit in column or row and one row or column bits of error will be corrected.

P81	P41	P21	P11	M11	M12	M13	M14	M15	M16	M17	M18
P82	P42	P22	P12	M21	M22	M23	M24	M25	M26	M27	M28
P83	P43	P23	P13	M31	M32	M33	M34	M35	M36	M37	M38
P84	P44	P24	P14	M41	M42	M43	M44	M45	M46	M47	M48
.	.	.	.	M51	.	.	.	.	.	.	M58
.	.	.	.	M61	.	.	.	.	.	.	M68
.	.	.	.	M71	.	.	.	.	.	.	M78
P88	P48	P28	P18	M81	M82	M83	M84	M85	M86	M87	M88
				Q11	Q12	.	.	.	.	.	Q18
				Q21	Q22	.	.	.	.	.	Q28
				Q41	Q42	.	.	.	.	.	Q48
				Q81	Q82	.	.	.	.	.	Q88

Figure (4). Parity and message in two dimension mode

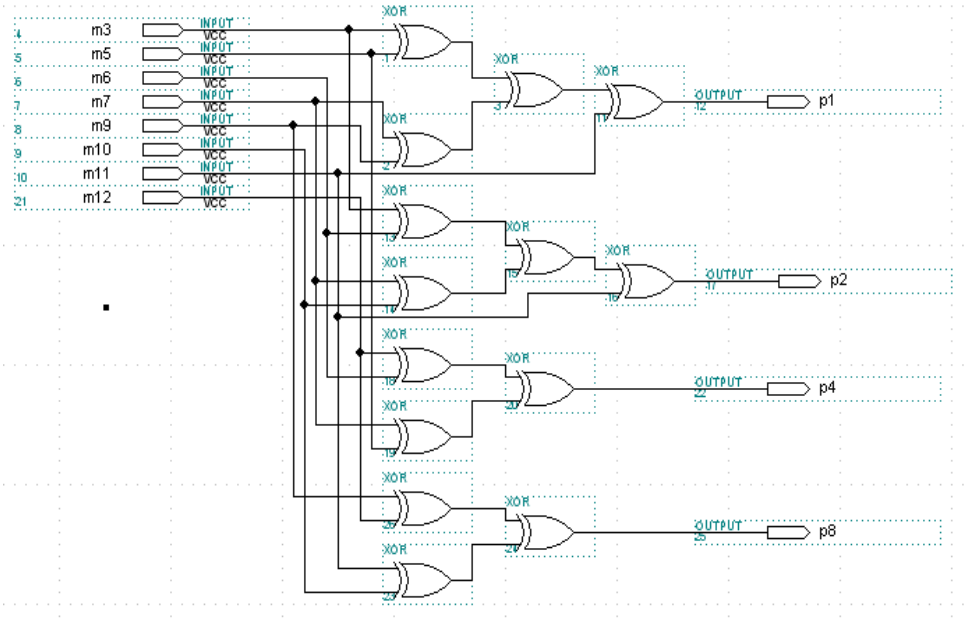

Figure (5). Parity bit generator circuit

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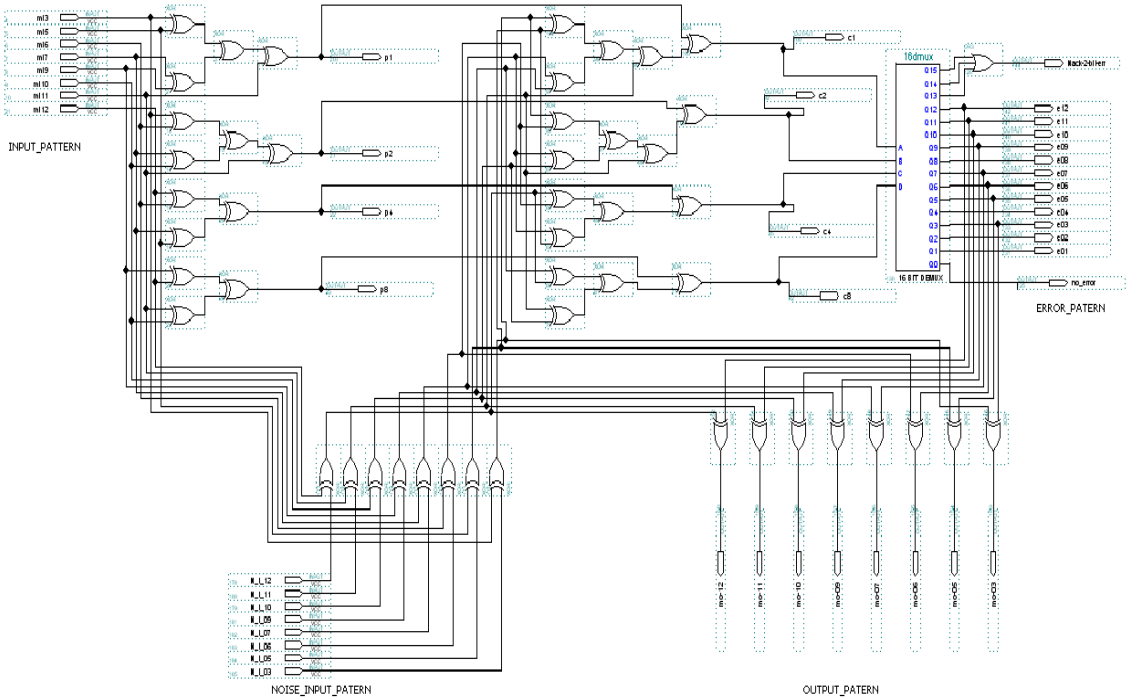

Figure (6). Error correction circuit with test circuit

If error bite have 2 or higher error bit in a both of row and column then it is not possible to correct this errors. In other diction if we have shadow error bits on both of row and column then it is not possible to correct errors and only can detecting those error bits. Based on equations from (1) to (4) the error correction and detection circuits are designed and shown in figures (5) and (6) that parity bits generated with XOR gates and store to register. The errors will be corrected if possible and if not possible the output of correction circuit of shown in figure (6) will activated and if corrected will be stored in register.

By showing this circuit with block diagram then show this circuit in row and column separately then figure (7) show this block diagram.

IV. CONTROL OF POWER IN TWO DIMENSIONAL CIRCUIT DYNAMICALLY

For decrease of power consumption must power off some party of circuit that shown in figure (7). It is possible that measurement the power level of power supply and manage correction and detection circuit and parity generator circuit in both of sender and receiver circuits. By decrease of power level of power supply the number of bits that can be corrected or detected and the power consumption will be decreased. This is done with the AND gated that shown in figure (7) beside the power manager block diagram.

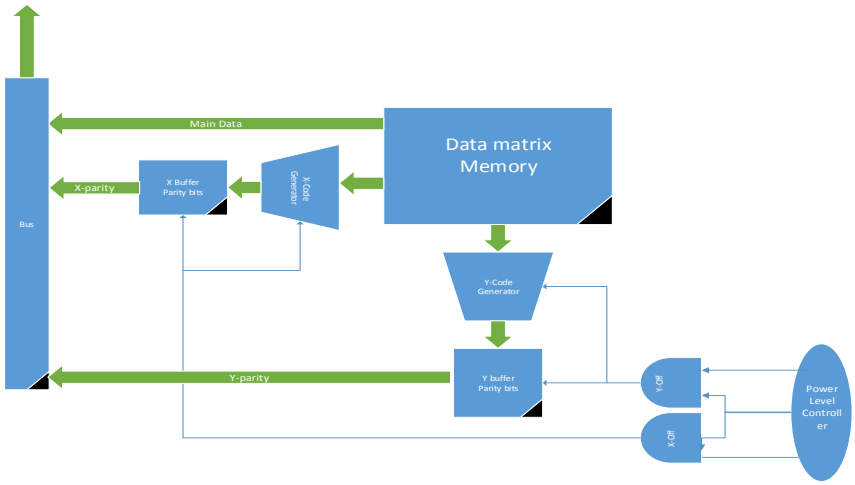

Figure (7). Two dimensional Error correction and detection block diagram in power aware state

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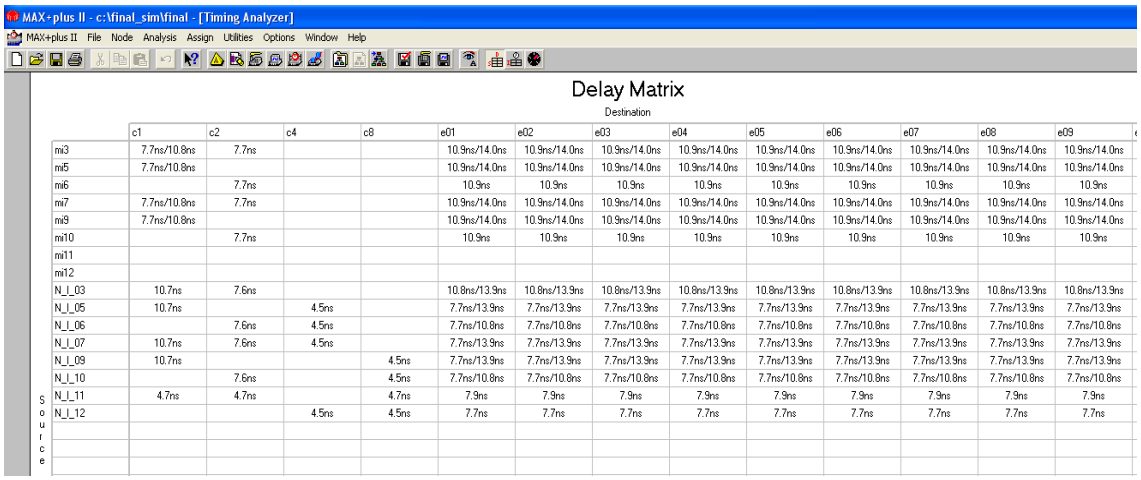
Both of sender and receiver are synchronous for power detecting level and if one of the sender or receiver be decrease this power level then both of sender and receiver decrease the power consumption for doing same protocol in sender and receiver. For synchronous of sender and receiver we need two bit that separate state of those bits are introduce.

- (00) State: in this state the energy level is very low and error correction will not be done.
- (01) State: in this state the energy level is fair and error correction will be done in one dimension X.
- (10) State: in this state the energy level is good and error correction will be done in both dimension X and Y. in this state maximum error correction will be done.

Therefore the state level selecting is done by equation (6). In this state we know that both of sender and receiver must select minimum state of power of each other for power aware done correctly.

$$Level\ Select = Min\{Tx\ Level, Rx\ Level\} \quad (6)$$



	c1	c2	c4	c8	e01	e02	e03	e04	e05	e06	e07	e08	e09
mi3	7.7ns/10.8ns	7.7ns			10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns
mi5	7.7ns/10.8ns				10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns
mi6		7.7ns			10.9ns	10.9ns	10.9ns	10.9ns	10.9ns	10.9ns	10.9ns	10.9ns	10.9ns
mi7	7.7ns/10.8ns	7.7ns			10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns
mi9	7.7ns/10.8ns				10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns	10.9ns/14.0ns
mi10		7.7ns			10.9ns	10.9ns	10.9ns	10.9ns	10.9ns	10.9ns	10.9ns	10.9ns	10.9ns
mi11													
mi12													
N_I_03	10.7ns	7.6ns			10.8ns/13.9ns	10.8ns/13.9ns	10.8ns/13.9ns	10.8ns/13.9ns	10.8ns/13.9ns	10.8ns/13.9ns	10.8ns/13.9ns	10.8ns/13.9ns	10.8ns/13.9ns
N_I_05	10.7ns		4.5ns		7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns
N_I_06		7.6ns	4.5ns		7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns
N_I_07	10.7ns	7.6ns	4.5ns		7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns
N_I_09	10.7ns			4.5ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns	7.7ns/13.9ns
N_I_10		7.6ns		4.5ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns	7.7ns/10.8ns
N_I_11	4.7ns	4.7ns		4.7ns	7.9ns	7.9ns	7.9ns	7.9ns	7.9ns	7.9ns	7.9ns	7.9ns	7.9ns
N_I_12			4.5ns	4.5ns	7.7ns	7.7ns	7.7ns	7.7ns	7.7ns	7.7ns	7.7ns	7.7ns	7.7ns

Figure (8). Simulator conclusion

In this state if only one of the senders energy level come down then receiver and other senders that connect to this receiver will work in level of minimum of the network. In other way we can say that the minimum energy of system is appointment by minimum energy of every sender or receiver of all connected systems.

Both of Tx or Rx level can be determined by (00), (01) or (10) that show the energy level of own system.

V. SUMMARY AND CONCLUSIONS

After simulating with maxplusII software for error detection and correction of above circuits and intern of error to system for test the result was shown in figure (8).

In Figure (8) we can see the errors that corrected after about 11 ns on e08 column. Number of column are blank for wait to other dimension correct this error.
In the (00) state the system could not detect and correct the errors and all of column will be blank.

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